## REMARKS

### I. Present Status of the Application

The Office Action mailed February 4, 2005 rejected all pending claims 1-4. Specifically, claims 1-4 were rejected under 35 U.S.C. 103(a) as being unpatentable over Torelli et al. (US 6,366,496). In response thereto, Applicants have amended independent claims 1 and 3. Reconsideration of claims 1-4 is respectfully requested.

### II. Response to Rejections under 35 U.S.C. 103(a)

Please refer to amended independent claims 1 and 3, one feature of this invention is that an additional programming voltage is applied after the normal programming voltage, wherein the additional programming voltage is ***capable of adjusting the state*** programmed by the normal programming voltage. According to the embodiment illustrated in FIG. 3 of this invention, for example, the additional programming voltage (1shot PGM) is not a programming ***verify*** voltage, but is one applied after a programming verify voltage (PV3).

Meanwhile, according to paragraph [0026], the application of the additional programming voltage can, for example, ensure that the reading current at the highest state is precisely within design limits. Therefore, the amendment that *the additional programming voltage is capable of adjusting a state of the memory* can be supported.

Torelli et al. fail to teach or suggest the above feature of this invention. As mentioned in Page 2 of the Office Action and clearly shown in FIG. 7 of Torelli et al., the voltage ($V_V$) considered as an additional programming voltage in the Office Action is actually a programming

***verify*** voltage that is also applied in this invention (e.g., PV1-PV3 in FIG. 3). Since $V_V$ ( FIG. 7 of Torelli et al.) is much lower than the programming voltages ($V_P$), $V_V$ is applied merely for detecting whether the cell has been correctly programmed to the required state or not, i.e., for ***verifying*** the state of the cell, ***but is not capable of adjusting the state.*** Therefore, the additional programming voltage as mentioned in claim 1 or 3 should be sufficiently distinguishable from the programming verify voltage ($V_V$) of Torelli et al., ***even in claim language.***

Accordingly, at least the above feature of this invention, *the step of applying an additional programming voltage capable of adjusting a state of the memory*, is not taught, suggested or implied in Torelli et al.

For at least the above reasons, Applicants respectfully submit that independent claims 1 and 3 and claims 2 and 4 dependent therefrom patently define over the prior art.

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## CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-4 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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